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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,988	08/06/2003	Mitsumi Ito	61282-035	7469

7590 07/28/2005

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,988	ITO ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-15,17 and 18* is/are rejected.

7)☒ Claim(s) *9-12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/5/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasagawa (US Patent 6,748,574) in view of Smith et al. (US Patent Application Publication 2003/0229875).

2. As for claims 1, 4, and 13, (claim 13 having similar limitations as claim 1), Sasagawa discloses the invention substantially as claimed, including a method of generating a pattern for a semiconductor device comprising:

A step of designing and arranging a layout pattern of a semiconductor chip [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28];

A step of extracting an area ratio of the layout pattern [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28];

A step of determining a most appropriate area ratio of the layout pattern of a layer according to a design rule of the layer [abstract, col. 3, lines 54-60].

Sasagawa does not specifically disclose a step of adding and arranging a dummy pattern to the layout pattern, so that the area ratio of the layer can be the most appropriate ratio

Smith discloses a step of adding and arranging a dummy pattern to the layout pattern for the purpose of improving density ratios [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sasagawa and Smith because adding Smith's dummy patterns to Sasagwa's method of determining optimal density of a layout would provide a way of ensuring uniform distribution of elements for planarization therefore improving semiconductor manufacturing processes [see Smith fig. 32, and pg. 16 paragraph 0255].

[claim 4], Sasagawa further discloses wherein an area ratio after the completion of forming the dummy pattern is calculated, it is judged whether or not the area ratio is in a range of a predetermined condition, and when the area ratio is not in the range of the predetermined condition [abstract, col. 3 – col. 4, especially col. 3, lines 54-60].

Sasagawa does not specifically disclose several of the dummy patterns are replaced and the most appropriate dummy pattern cell is selected.

Smith discloses several of the dummy patterns are replaced and the most appropriate dummy pattern cell is selected [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sasagawa and Smith because replacing dummy patterns with the most appropriate dummy pattern cell would provide a way of ensuring uniform distribution of elements for planarization therefore improving semiconductor manufacturing processes [see Smith fig. 32, and pg. 16 paragraph 0255].

3. Claims 2-3, 5-8, 14-15, and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasagawa (US Patent 6,748,574) in view of Smith et al. (US Patent Application Publication 2003/0229875) and further in view of Asakawa (US Patent Application Publication 2002/0157076).

4. As for claims 2-3, 5-8, 14-15, and 17-18, Sasagawa in view of Smith further discloses dividing the layout pattern, extracting an area ratio for each small region, adding a dummy pattern, preparing a plurality of types of dummy pattern cells, selecting a desired dummy pattern according to the area ratio of the small region, a wiring layer pattern, a diffusion layer, gate electrode, a well, and a well [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28; also figs. 1a-b, 2a-b, 5a-b, 6a-b, 11, 14-15, 22a-b, 23, paragraphs 0179, 0186, 0192-0201, 0206, 0215, 0235-0237, 0255, 0259, 0262].

Sasagawa in view of Smith does not specifically disclose using a mask pattern and the actual device made from the design process.

Asakawa discloses a semiconductor device formed by using a mask [paragraph 0037].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Sasagawa in view of Smith and Asakawa because both Sasagawa in view of Smith and Asakawa are directed towards the design and manufacture of semiconductor devices through the use of dummy patterns, and adding Asakawa's use of masks to manufacture a semiconductor device would have allowed Sasagawa in view of Smith's design to utilize well known techniques to manufacture the designed semiconductor after design was complete [see Asakawa, paragraph 0037].

5. Claims 9-12, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination the invention as claimed including a method of generating a pattern for a semiconductor device including at least a step of adjusting a layout in the vertical direction so that the dummy pattern cell can compose an MOS capacitor cell; or a semiconductor device wherein the pattern for a semiconductor device has an aggregation of dummy patterns of the same size not to be electrically connected, and at least one of the dummy patterns on each layer includes a region overlapped with a dummy pattern on an upper or a lower layer of the layer concerned in the vertical direction.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner

Art Unit 2825

SAW

July 24, 2005